PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Lea et al.	)	Examiner: Peter L. Cheng
Serial No.: 10/669,247	)	Art Unit: 2625
Filed: September 24, 2003	)	Confirmation No.: 3532
For: **System and Method of Parallel Processing Image Data** **(as amended)**	)	
Date of Examiner's Answer November 18, 2008	)	Attorney Docket No.: 200207569-1

January 19, 2009

REPLY BRIEF under 37 CFR §41.41

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Reply Brief is timely provided within two months from the mailing date of the Examiner's Answer dated November 18, 2008.

Reply

In response to the Examiner's Answer, dated November 18, 2008, Appellant respectfully submits the following reply as permitted under 37 CFR §41.41(a)(1). The Examiner's Answer contained no new grounds of rejection and the present reply contains no new amendment, affidavit or other evidence. Thus a formal Brief is not required. The present reply supplements Appellant's Appeal Brief in view of the Examiner's Answer.

The following sections address the Examiner's Answer and the section "(10) Response to Argument" starting on page 25. Citations to page numbers from the Examiner's Answer will be referred to as "EA __".

I. Whether claims 1-4, 6-8, 10-12, 16-20, 22 and 23 are unpatentable under 35 U.S.C. 103(a) as being obvious over Shishizuka in view of Westervelt.

Claim 1

Regarding the claimed "page frame memory," the examiner's reply cites to a FIFO buffer discussed in Shishizuka col. 44, lines 14-18 (EA page 26). Although not stated in the reference, a FIFO buffer is assumed to be a First In, First Out buffer as is commonly known for "FIFO". The cited section refers to figure 77, which shows the components of a FIFO controller 6603. The controller 6603 includes a "PRINTER FIFO 7701". The examiner states that this FIFO is separate from the "cache memory 403" and is connected to the GBI interface (EA page 26, 2nd and 3rd paragraphs). The examiner thus concludes that these components teach the claimed recitation of components and connections. However, they do not.

In particular, claim 1 recites:

a page frame memory configured to store a page of data, copied from the memory, that is to be imaged;

None of the cited sections or the FIFO 7701 teach a "page frame memory" that stores "a page of data" or that the page of data is "copied from the memory". As claim 1 specifies, the memory stores "image data as a page of data" that is generated from the scanner.

The FIFO 7701 is not a "page frame memory" that stores a "page of data" as claimed. Shishizuka explains that FIFO 7701 only holds 64 bits of data: "FIFO 7701 which has a capacity of 512 bytes (64 bits_64)." (col. 44, lines 18-19). As is known in the art, it is impossible for a "page of data" that comes from a scanned image to fit in a 512 byte capacity buffer. The present specification describes example pages of data as "a 105 MB [megabyte] color page", which after compression may be 21 megabytes (page 6, [0021], "21 MB"). The present specification also describes the page frame memory in terms of megabytes as being "64 MB" to store "a single compressed page" (page 6, [0023]). Therefore, one of ordinary skill in the art would not understand the FIFO buffer 7701, which holds only 512 bytes, to be a "page frame memory" that can store "a page of data" as claimed. The FIFO buffer is not configured to store a page of data and does not provide the function of storing a page of data. Even more relevant is that none of the components, circuits or busses that use the FIFO buffer 7701 is configured to process a "page of data" as a unit or store a page of data in the FIFO buffer 7701.

Thus the claim is not taught or suggested and the rejection should be reversed.

Regarding Westervelt, the examiner relies on the reference for teaching that the size of the printer FIFO of Shishizuka can be made bigger (EA page 37, 4th paragraph). However, it is not obvious to increase the size of the printer FIFO in

Shishizuka because Shishizuka explicitly teaches that the printer FIFO has a "capacity" of 512 bytes: "FIFO 7701 which has a capacity of 512 bytes (64 bits_64)." (col. 44, lines 18-19). Therefore, the purpose and function of the FIFO 7701 is not to store "a page of data". Shishizuka does not explicitly describe the purpose of FIFO 7701. However considering its very small size, one of ordinary skill in the art would understand that the function of FIFO 7701 is simply to buffer small streams of bits, and is not for storing a page of data. One of ordinary skill would not find it obvious to replace a 512 byte capacity buffer with one that has a capacity to store a page of data, which could be megabytes greater in size (millions of times larger) (present specification [0022]). Such a modification contradicts the intended purpose of the FIFO buffer 7701 and thus would change its principle of operation. This is an improper modification according to MPEP 2143.01 and thus not obvious.

Furthermore the issue here is not merely about changing size as the examiner states (EA page 37). Even if the size of the FIFO buffer were changed, the FIFO buffer 7701 (fig. 77) would still not function to store "a page of data." A "page of data" is a specific unit of data that has a definite beginning and end, namely the beginning of a page and the end of a page. The circuit of Shishizuka is configured to process small bits of data (512 bytes) that stream through the FIFO buffer 7701 (col. 44, lines 18-19). The proposed modification cannot simply change the size of the FIFO buffer to achieve the claimed feature because the entire circuit of figure 77 is designed to and will still operate by processing 512 byte (64 bit) streams to the FIFO. Simply using a larger FIFO buffer does not change the operation of the other circuit components. A larger FIFO in figure 7 does not perform the same function as the buffer from Westervelt and is thus not obvious under MPEP 2143(A)(2).

Additionally, a modification to make FIFO 7701 configured to process a page of data would require significant reconfiguration to all circuits, busses, and

components that function with the FIFO 7701. For example with regard to figure 77, the prcDataIn bus would have to be reconfigured to process a page of data rather than 64 bits. The same would occur with the RDATA bus out from the FIFO 7701. Any downstream components that receive the 64 bits from the RDATA bus would be expecting to receive 64 bits, not a page of data. It is well known in data processing arts that when the format of an expected signal is changed, an error occurs in the receiving component because the new signal is not understood. No evidence has been presented in the rejections that teach or suggest such modifications to these components. Thus the proposed modification is not obvious.

Further looking at figure 77, the Arbitrator circuit 7702 would also need to be reconfigured to process "a page of data" rather than streaming 512 bytes. The Arbitrator 7702 does not process "a page of data" and no reference has been cited to suggest that it is obvious to modify the Arbitrator 7702 in such a manner.

The proposed modification would further need to be propagated throughout all components that communicate with the circuit of figure 77. For example, the printer video clock unit 6802 controls when data is outputted to the FIFO by issuing a request (col. 44, lines 22-23). Thus the clock unit 6802 would need to be reconfigured to issue requests to handle a page of data. The timing of the request would need to be reconfigured somehow. There is no teaching or suggestion to make this modification or how to make this modification.

The reconfigurations then must continue to other affected components like the circuit of figure 68 that is connected to and functions with the clock unit 6802 and so on. Therefore, the proposed modification of simply changing the size of FIFO buffer 7701 (1) still fails to teach or suggest the claimed features because the circuit still does not process a page of data or teach the bus configuration, and (2) the modification ignores the requirements of the affected circuits and fails to consider the disclosure as a whole and how the system operates. Modifying all the

circuits to process a page of data would change the principle of operation of the prior art invention being modified. Thus the teachings of the references are not sufficient to render the claims *prima facie* obvious. MPEP 2143.01 (VI) citing *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959). The modification is not obvious and is improper. The rejections should be reversed.

Appellant repeats the arguments regarding the claimed dual bus system as stated in the Appeal Brief (pages 11-14).

Overall, claim 1 recites a configuration of components and a dual bus system that is significantly more simple and elegant than the highly complex system of Shishizuka that has thousands of components over 118 figures. The references fail to teach or suggest a bus system with the features and functions of the claimed dual bus system. This has been explained in detail above and in Appellant's Appeal Brief.

Independent Claim 11

The reply to claim 11 starts on EA page 39. The reply relies on Shishizuka's VSYNC and HSYNC Timing Signals. The irrelevance of the VSYNC and HSYNC signals was explained in Appellant's Appeal Brief pages 14-15 and 17. Therefore each and every element of claim 11 is still not taught or suggested by the combined references. The reliance on Westervelt is insufficient to teach the claimed elements for the reasons stated above under claim 1 and in the appeal brief. A prima facie obviousness rejection has not been established and the rejection should be reversed.

Independent Claim 17

The reply to claim 17 simply cites to claims 1 and 2 (EA page 40). Appellant repeats the arguments of the appeal brief. The rejection should be reversed.

II. Whether claims 5, 9, 13, 14, 15 and 21 are unpatentable under 35 U.S.C. 103(a) as being obvious over Shishizuka (US Patent 6,697,898 B1), in view of Westervelt (US Patent Appl. 2003/0231330 A1), in view of well-known prior art.

The examiner cites MPEP 2144.03 and claims that the appellant has failed to adequately traverse the position of common knowledge (EA page 41). In particular, the examiner cites MPEP 2144.03, paragraph C. The examiner's interpretation of paragraph C is incorrect. The title of paragraph C states:

> **C. If Applicant Challenges a Factual Assertion as Not Properly Officially Noticed or Not Properly Based Upon Common Knowledge, the Examiner Must Support the Finding With Adequate Evidence**

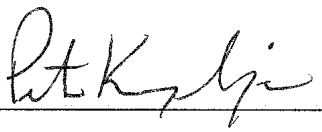
The applicant's requirement to adequately traverse such a finding only exists after (1) the applicant challenges the factual assertion and (2) after the examiner supports the finding with adequate evidence. In the present case, the applicant has challenged the factual assertion (see appeal brief page 19). Now the "Examiner must support the finding with adequate evidence" as stated in MPEP 2144.03 (C) (emphasis added), which has not been performed. Therefore, the common knowledge assertion has not been supported with adequate evidence and is improper. Applicant has not failed to adequately traverse the assertion since the requirement only exists after the examiner provides adequate evidence.

Appellant repeats the reasoning submitted in the Appeal Brief. A prima facie anticipation or obviousness rejection has not been established. The rejection should be reversed.

Conclusion

Appellant respectfully maintains all previous arguments, which show the deficiencies in the rejections, along with the additional comments submitted herein. Accordingly, Appellant respectfully requests that the Board of Appeals overturn all rejections and allow all pending claims.

Respectfully submitted,



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